Title: Using HLS in Digital Radar Frontend FPGA-SoCs

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Content of presentation:

For avionic sensor equipment there is a strong persistent trend to smaller **S**ize, **W**eight **A**nd more **P**ower/**c**ost efficient systems (SWAP-c). Additionally there is a desire for multifunctional sensors where software-defined radio concepts have to be applied. Further digitalization of radar frontends means, beside increasing the sampling rate of ADCs, for example using digital beamforming which further increases the amount of data to be handled at the frontend. The samples have to processed continuously in real time and this is where FPGAs come into play.

With the advent of High-Level Synthesis (HLS) it became possible to implement very complex algorithms in FPGAs in an efficient way. Because of the high dynamic range of radar signals, the numerical accuracy is more demanding than in mobile communication systems. Thus, for radar applications, a floating-point implementation can be reasonable which is also supported by HLS. This presentation will give an overview how FPGA-SoCs can be efficiently used for digital radar frontends. It will focus on the consideration which parts of the design are suitable to be designed with HLS and where the traditional HDL way makes more sense. The acceleration of design productivity using HLS and its limitations will be discussed. The partitioning of functions in programmable logic and software functions will be touched as well.